

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. 1. A method for modifying a diffusions rate of an impurity implanted in a semiconductor material including steps of
 - 4 defining a boundary with a structure on a surface of said semiconductor material,
 - 5 applying a stressed film over said structure and said surface at said boundary, and
 - 6 annealing said semiconductor material to activate said impurities.
- 1 2. The method as recited in claim 1, wherein said structure on said surface of said semiconductor material is a gate structure of a field effect transistor.
- 1 3. The method as recited in claim 2, wherein said boundary is defined by a sidewall of said gate structure.
- 1 4. The method as recited in claim 3, wherein said sidewall is an offset spacer.
- 1 5. The method as recited in claim 3, wherein said sidewall is a source/drain spacer.

1 6. The method as recited in claim 2, wherein said
2 boundary is defined by a gate electrode of said gate
3 structure.

1 7. The method as recited in claim 1, further
2 including steps of
3 implanting extension impurities,
4 implanting source/drain impurities, and
5 implanting halo impurities.

1 8. The method as recited in claim 1 wherein a
2 plurality of said structures are provided on said
3 surface of said semiconductor material, further
4 including a step of
5 removing said stressed film from a selected
6 said structure prior to said annealing step.

1 9. The method as recited in claim 8, wherein said
2 plurality of structures include gate structures of
3 pFETs and nFETs.

1 10. The method as recited in claim 9, wherein said
2 boundary is defined by a sidewall of said gate
3 structures.

1 11. The method as recited in claim 10, wherein said
2 sidewall is an offset spacer.

1 12. The method as recited in claim 10, wherein said
2 sidewall is a source/drain spacer.

1 13. The method as recited in claim 1, wherein said
2 stressed film is a tensile film.

- 1 14. An intermediate structure for formation of a
- 2 semiconductor device, said intermediate structure
- 3 comprising
 - 4 a body of semiconductor material including
 - 5 respective regions implanted with boron and arsenic
 - 6 impurities,
 - 7 a structure on a surface on said body of
 - 8 semiconductor material and forming a boundary, and
 - 9 a stressed film extending over said structure
 - 10 and said boundary,
 - 11 wherein when said intermediate structure is
 - 12 annealed to activate said boron and arsenic
 - 13 impurities, a diffusion rate of said boron
 - 14 impurities is modified.
- 1 15. The intermediate structure as recited in claim
- 2 14, wherein said structure is a gate structure of a
- 3 field effect transistor.
- 1 16. The intermediate structure as recited in claim
- 2 15, wherein said gate structure includes a sidewall.
- 1 17. The intermediate structure as recited in claim
- 2 16, wherein said sidewall is an offset spacer.
- 1 18. The intermediate structure as recited in claim
- 2 16, wherein said sidewall is a source/drain spacer.

- 1 19. An integrated circuit comprising
- 2 a pFET, and
- 3 an nFET
- 4 wherein a boron diffusion concentration profile
- 5 from extension implants in said pFET corresponds to
- 6 a lower boron diffusion rate than a boron diffusion
- 7 rate corresponding to a boron diffusion
- 8 concentration profile from a boron halo implant in
- 9 said nFET.

- 1 20. A pFET including
- 2 a source/drain region formed by implantation
- 3 with boron, and
- 4 an extension region formed by implantation with
- 5 boron, wherein a boron concentration profile of said
- 6 extension in a lateral direction differs from a
- 7 boron concentration in a vertical direction.